SYM53C710 to SYM53C770 Comparison

System Engineering Note

S11004

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Revision History

First revision, 6/99

1 Introduction

This document compares contrasts the SYM53C710 and SYM53C710 to provide users with a mechanism to improve transition from the older chip to the newer. The differences are covered in the subsequent sections of the document:

Section 2, “Features”

Section 3, “Host Bus Interface Differences”

Section 4, “SCRIPTS Instruction Differences”

Section 5, “SCSI Bus Interface Differences”

Section 6, “Register Differences”

2 Features

This section of the document provides a high level overview of the differences between the SYM53C710 and SYM53C770. Table 1 compares the two chips and provides the overview.

Table 1 SYM53C710 to SYM53C770 Overview

FEATURES	SYM53C710	SYM53C770
SCSI Data Transfer Rate Synchronous	10 Mbytes/s	40 Mbytes/s
Internal Ram for SCRIPTS	None	4KB
Variable Block sizes and scatter/gather	Supported	Supported
Data bursts with variable burst lengths	32-bit	16- and 32-bit
DMA Transfer Rate	66 Mbytes/s	105 Mbytes/s
Performs complex bus sequences with out interrupts, including restoring data pointers	Not Supported	Supported
Performs memory transfers in excess of 100MB/s	Not Supported	Supported
DMA FIFO (cache line bursting)	64-byte	96-byte
SCSI Offset	8 levels	16 levels
Odd-byte block size in conjunction with Wide SCSI	Not Supported	Supported
SCSI Clock Double	Not Supported	Supported
Fairness Timer	5-8 CLKs	5CLKs
Host Bus Width	32 bits	16 or 32 bits
SCSI Bus Width	8 bits	8 or 16 bits
Interrupt On-The-Fly	Not Supported	Supported
Bus Modes	4	7
SCRIPTS Auto-Start	Not Supported	Supported
Programmable Burst Length	1, 2, 4 or 8	2, 4, 8 or 16
Shadowed Temp and DSA Registers	Not Supported	Supported

Table 1 SYM53C710 to SYM53C770 Overview

FEATURES	SYM53C710	SYM53C770
Programmable SCSI Timers	Not Supported	3
General Purpose I/O Pins	Not Supported	Supported
Differential Sense Pin	Not Supported	Supported
Preview of Next Address	Not Supported	Supported
Carry Bit In ALU	Not Supported	Supported
Semaphore Bit	Not Supported	Supported
Devices on SCSI Bus	8	16
Host Parity Checking	Not Supported	Supported

3 Host Bus Interface Differences

The SYM53C770 host bus interface has been significantly enhanced in relation to the bus for the SYM53C710. By allowing the SYM53C770 to interface directly with a larger number of host busses, greater flexibility and functionality is provided. The SYM53C770 is still compatible signal for signal with the SYM53C710 host bus interface. This section of the document provides descriptions of the host bus interface differences listed below.

Section 3.1, “Bus Mode Select Pins”

Section 3.2, “Enhanced Cache-Line Burst”

Section 3.3, “Sense Pin for SCRIPTS Auto-Start”

Section 3.4, “General Purpose Input and Output Pins”

Section 3.5, “Memory Access Control Pin”

Section 3.6, “Test In and Test Out Pins”

3.1 Bus Mode Select Pins

The SYM53C770 interfaces with host busses in a combination of the following modes: Motorola or Intel, Big or Little Endian, 68040_68030, or 80386dx_80386sx. If Intel and one of the 80386 modes are selected, several pins change functions. In particular the R_W/ pin becomes inverted and SIZ0, SIZ1, A0 and A1 become byte enable signals. The SYM53C710 is only capable of interfacing with host busses in a combination of the following modes without external hardware: Big or Little Endian, 68030, or 68040.

3.2 Enhanced Cache-Line Burst

Cache-Line Burst eliminates the need for a full handshake between the SYM53C770 bus and the memory device when transferring data. The bus master arbitrates for the bus at the beginning of a 16-byte transfer and can transfer one long word per clock period. The SYM53C770 starts another Cache Line Burst without getting off the bus if it has another 8 long words stored in its FIFO. Under optimal conditions, the SYM53C770 will have 16 long words in its FIFO. This allows it to do four back-to-back cache transfers. A Cache Line Burst is always 4 long words in length. The SYM53C710 was only capable of doing one Cache Line Burst before surrendering the bus.

Cache-Line Burst mode allows up to 105 Mbytes/s DMA burst bandwidth for extremely high data transfer rates or streaming modes. The SYM53C710 is only capable of 66 Mbytes/s DMA transfers.

3.3 Sense Pin for SCRIPTS Auto-Start

When the SCRIPTS auto-start sense pin is tied to ground the DMA SCRIPTS Pointer Register (DSP) points to an address of all zeros. The SCRIPTS processor starts fetching instructions from that location. If the sense pin is tied high, the DSP register must be written with the starting address of the first SCRIPTS instruction.

The auto-start feature enables the SYM53C770 to start the SCRIPTS program automatically after reset is deasserted. SCRIPTS instructions are fetched and executed until an interrupt condition occurs.

3.4 General Purpose Input and Output Pins

The SYM53C770 has four input and one output pins. These pins are user defined. The input pins can be used to read the SYM53C770 chip ID or other configuration information. The output pin can be used to enable on-board ROM, RAM or LEDs.

3.5 Memory Access Control Pin

The signal on this pin indicates whether the next access is to near memory (local, on-board) or far memory (system). The ability to select either near and far memory provides system design flexibility and faster local memory data access.

3.6 Test In and Test Out Pins

These pins connect all inputs and outputs, excluding SCSI control signals and data lines, to an AND tree test scheme. This function allows manufacturers to verify chip connectivity to the board and to determine exactly which pins are not properly attached.

4 SCRIPTS Instruction Differences

Six SCRIPTS instructions have been added to the SYM53C770. The SYM53C770 utilizes all of the SCRIPTS instructions available for the SYM53C710, therefore, SCRIPTS programs developed for the SYM53C710 are upward compatible. For a more detailed description of the SCRIPTS language, reference the SYM53C720/se/SYM53C770 Programmer's Guide. The sections listed below provide a brief description of the new instructions.

Section 4.1, “CHMOV Instruction”

Section 4.2, “INTFLY Instruction”

Section 4.3, “Transfer Control Instruction on Carry”

Section 4.4, “Read/Write Instruction With Carry Enabled”

Section 4.5, “Read/Write Instruction With Use data8/SFBR Enabled”

Section 4.6, “I/O Instruction SET or CLEAR Carry”

4.1 CHMOV Instruction

The CHMOV instruction transfers data to and from memory locations. Data may come from any data location, so scatter/gather operations are transparent to the chip and the external processor.

When the SYM53C770 executes several CHMOV instructions and one ends on an odd byte boundary, the SYM53C770 temporarily stores the residual byte. It takes the first byte from the subsequent CHMOV or MOVE instruction and lines it up with the residual byte in order to complete a wide transfer and maintain a continuous data flow of the SCSI bus.

4.2 INTFLY Instruction

The INTFLY instruction (DBC, bit 20) asserts the Interrupt on the Fly bit (ISTAT, bit 2) after executing the SCRIPTS instruction. SCRIPTS programs do not halt when the interrupt occurs.The interrupt can only be serviced by reading the Interrupt Status Register. The INTFLY instruction notifies a service routine, running on the main processor, while the SCRIPTS processor is still executing a SCRIPTS program.

4.3 Transfer Control Instruction on Carry

Jump, Call, Return, or Interrupt can be executed after an add operation, depending on the resulting carry bit (DBC, bit 21). hen executing a transfer control instruction true/false comparisons are legal whereas compare functions are illegal. For example, INT address, IF carry and INT address, IF NOT carry are legal. The transfer control on carry feature adds additional flexibility to the user by allowing additions to cross byte boundaries.

4.4 Read/Write Instruction With Carry Enabled

When carry is enabled (DCMD, bit 0) any read/write opcode utilizing the add operation also adds in the current carry contents. MOVE SCRATCH1 + 1 To SCRATCH1 WITH Carry, is an example. Enabling the carry bit allows the SYM53C770 to perform add operations greater than one byte, since carry values from previous byte adds may be used in successive adds.

4.5 Read/Write Instruction With Use data8/SFBR Enabled

When set, the SFBR is used instead of the data8 value during the Read-Modify-Write instruction. This enables the user to operate on two registers. This bit was a reserved bit for the SYM53C710.

4.6 I/O Instruction SET or CLEAR Carry

The Carry bit may be SET or CLEARed using a SCRIPTS Instruction (DBC, bit 10). This feature permits the user to assert or deassert the carry bit prior to an addition or subtraction operation.

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5 SCSI Bus Interface Differences

The primary difference between the SYM53C710 and the SYM53C770 is Wide SCSI implementation. The differences in Wide SCSI implementation are described in the sections listed below.

Section 5.1, “Wide SCSI”

Section 5.2, “Differential Sense Pin”

Section 5.3, “SCSI Clock”

Section 5.4, “Initiator/Target Auto-Switch Disabled”

Section 5.5, “SCSI Timers”

Section 5.6, “Separation of Selection and Reselection Control”

5.1 Wide SCSI

The SYM53C770 has a 16-bit data transfer capability. There is a single request/acknowledge per transfer and the SCSI bus pinout is optimized for P or A cable connection.

Note: The upper SCSI lines must be terminated even if the SYM53C770 is used with an 8-bit SCSI bus.

Wide SCSI provides a significant increase in system performance especially in systems requiring large data transfers between host and peripheral devices. The SYM53C770, with Wide SCSI, transfers data at

up to 40 Mbytes/s whereas the SYM53C710 transfers are limited to 10 Mbytes/s. This comparison is only true when the SCSI bus is operating in synchronous and differential modes.

5.2 Differential Sense Pin

The SYM53C770 uses the Differential Sense pin to determine if a connected SCSI device is operating in differential or single ended mode. If the external device is operating in differential mode while the SYM53C770 is in single ended mode, the chip ceases to drive external outputs on the SCSI bus. The differential sense pin must be pulled high for single ended operation. The sense pin protects the external differential pair transceivers and the single ended device from damage.

5.3 SCSI Clock

The SYM53C770 has a separate SCSI clock, operating at up to 100 MHz. This is twice the speed of the SYM53C710 clock, at up to 50 MHz.

Separate SCSI and bus clocks allow the host interface to operate at a lower speed while a higher speed clock controlling the SCSI bus guarantees fast SCSI timings of 20 Mbytes/s. A clock speed of minimum 40 MHz is required for fast SCSI.

5.4 Initiator/Target Auto-Switch Disabled

The auto-switch function is disabled in the SYM53C770. This forces the user to manually set target or initiator mode in a SCRIPTS program. It removes any ambiguity about SYM53C770 mode.

5.5 SCSI Timers

The SYM53C770 provides programmable select/reselect, handshake to handshake, and general purpose timers. The time-out period is programmable from 100 µs to 1.6 seconds. A maskable interrupt is available for each of the timers. The timers allow the user to tailor SCRIPTS instructions to their specific time-out needs.

5.6 Separation of Selection and Reselection Control

The SYM53C770 can be enabled to respond as a target, initiator or both. Status and interrupt bits indicate whether the SYM53C770 has responded to selection or reselection.

The SYM53C770 knows whether to respond as an initiator or a target. If the user has disabled selection and another SCSI device attempts to select the SYM53C770, the SYM53CU98 notifies the main processor.

6 Register Differences

The following sections summarize the differences between the SYM53C710 and the SYM53C770 register sets:

Section 6.1, “New Registers/Bits”

Section 6.2, “Deleted Registers/Bits”

Section 6.3, “Moved Registers/Bits”

For a more detailed explanation of each of the registers in the SYM53C770, reference the SYM53C720/*se*/SYM53C770 Data Manual.

Note: In the tables, registers are in bold type and bits in normal type.

6.1 New Registers/Bits

Table 2 summarizes the new registers added to the SYM53C770. The register and bit additions, as well as the resulting benefits to the user, are briefly described after the Table 2. For more precise descriptions of

each register or bit, refer to the register descriptions in the SYM53C770 Technical Manual.

Table 2 New Registers

Registers/Bits	SYM53C710	SYM53C770
Start SCSI Transfer bit	Not Supported	SCNTL1, bit 0
Immediate Arbitration bit	Not Supported	SCNTL1, bit 1
SCSI Control Register Two – 02h	Not Supported	SCNTL2
Wide SCSI Receive bit	Not Supported	SCNTL2, bit 0
Vendor unique Enhancements Bit	Not Supported	SCNTL2, bit 2
Wide SCSI Send bit	Not Supported	SCNTL2, bit 3
Chained Mode bit	Not Supported	SCNTL2, bit 6
SCSI Disconnect Unexpected bit	Not Supported	SCNTL2, bit 7
SCSI Control Register Three – 03h	Not Supported	SCNTL3
Enable Wide SCSI bit	Not Supported	SCNTL3, bit 3
Enable Response to Selection bit	Not Supported	SCID, bit 5
Enable Response to Reselection bit	Not Supported	SCID, bit 6
General Purpose Register – 07h	Not Supported	GPREG
General Purpose Inputs/Outputs	Not Supported	GPREG, bits 4-0
SCSI Selector ID Register – 0Ah	Not Supported	SSID
Encoded Destination SCSI ID Bits	Not Supported	SSID, bits 3-0
SCSI Selector ID Valid bit	Not Supported	SSID, bit 7
SCSI Parity SD 15-8 Bit	Not Supported	SSTAT2, bit 0
Last Disconnect bit	Not Supported	SSTAT2, bit 1
Latched SCSI Parity SD 15-8-Bit	Not Supported	SSTAT2, bit 3
SODL Most Significant Byte Full	Not Supported	SSTAT2, bit 5
SODR Most Significant Byte Full	Not Supported	SSTAT2, bit 6
SIDL Most Significant Byte Full	Not Supported	SSTAT2, bit 7

Table 2 New Registers

Registers/Bits	SYM53C710	SYM53C770
Interrupt On The Fly bit	Not Supported	ISTAT, bit 2
Semaphore bit	Not Supported	ISTAT, bit 4
Cache 386 Enable bit	Not Supported	CTEST0, bit 0
Generate Receive Parity for Pass Through	Not Supported	CTEST0, bit 4
Host Parity Check Enable bit	Not Supported	CTEST4, bit 3
Shadow Register Test Mode bit	Not Supported	CTEST4, bit 4
SCSI Data Bus High Impedance Mode	Not Supported	CTEST4, bit 5
Enable Host Parity Error Interrupt	Not Supported	DIEN, bit 6
Host Bus Width 16 bits	Not Supported	DCNTL, bit 3
Bus Mode bit	Not Supported	DCNTL, bit 6
Size Throttle Enable bit	Not Supported	DCNTL, bit 7
SCSI Interrupt Enable Register One 41h	Not Supported	SIEN1
Handshake Timer Expired	Not Supported	SIEN1, bit 0
General Purpose Timer Expired	Not Supported	SIEN1, bit 1
SCSI Interrupt Status Register Zero 42h	Not Supported	SIST0
SCSI Interrupt Status Register One 43h	Not Supported	SIST1
SCSI Wide Register 45h	Not Supported	SWIDE
Memory Access Control Register 46h	Not Supported	MACNTL
General Purpose Control Register 47h	Not Supported	GPCNTL
SCSI Time Register Zero 48h	Not Supported	STIME0
Programmable Select/Reselect Timer	Not Supported	STIME0, bits 3-0

Table 2 New Registers

Registers/Bits	SYM53C710	SYM53C770
Programmable Handshake Timer	Not Supported	STIME0, bits 7-4
SCSI Time Register One 49h	Not Supported	STIME1
SCSI Status Register Two	Not Supported	SSTAT2, bit 2
Response ID Zero Register 4Ah	Not Supported	RESPID0
Response ID One Register 4B	Not Supported	RESPID1
SCSI Test Register Zero 4Ch	Not Supported	STEST0
SCSI Synchronous Offset Max. bit	Not Supported	STEST0, bit 0
SCSI Synchronous Offset Min. bit	Not Supported	STEST0, bit 1
Arbitration Priority Test bit	Not Supported	STEST0, bit 2
Selection Response Logic bit	Not Supported	STEST0, bit 3
SCSI Test Register One 4Dh	Not Supported	STEST1
SCSI Test Register Two 4Eh	Not Supported	STEST2
Extended REQ/ACK Filtering bit	Not Supported	STEST2, bit 1
Always Wide SCSI bit	Not Supported	STEST2, bit 2
SCSI Control Enable bit	Not Supported	STEST2, bit 7
SCSI Test Register Three 4Fh	Not Supported	STEST3
SCSI FIFO Test Write bit	Not Supported	STEST3, bit 0
Clear SCSI FIFO bit	Not Supported	STEST3, bit 1
Timer Test Mode bit	Not Supported	STEST3, bit 2
16-bit System	Not Supported	STEST3, bit 3
Disable Single Initiator Response	Not Supported	STEST3, bit 4
Halt SCSI Clock bit	Not Supported	STEST3, bit 5

Table 2 New Registers

Registers/Bits	SYM53C710	SYM53C770
SCSI FIFO Test Read bit	Not Supported	STEST3, bit 6
TolerANT Enable	CTEST0, bit 4	STEST3, bit 7
SCSI Input Data Latch bits 15-8	Not Supported	SIDL
SCSI Output Data Latch bits 15-8	Not Supported	SODL
SCSI Bus Data Lines bits 15-8	Not Supported	SBDL
Scratch Register B 5C-5Fh	Not Supported	SCRATCHB
General Purpose Scratch Register C-J 60-7Fh	Not Supported	SCRATCHC-J

Note: Addresses are Little Endian.

Start SCSI Transfer Bit – The start SCSI transfer bit (SCNTL1, bit 0) has been added to initiate SCSI transfers. The SYM53C770 automatically sets the bit on execution of a transfer. Whether the transfer is send or receive is reflected by the value written to the I/O bit in the SCSI Output Control Latch Register. The SYM53C710 possessed two bits to indicate that the chip was starting a send or receive operation.

This bit is used for test purposes only and it is automatically set in low-level mode and during SCRIPTS execution.

Immediate Arbitration Bit – The SYM53C770 arbitrates immediately after a disconnect if this bit is asserted.

Immediate arbitration bit permits the SYM53C770 to participate in the next arbitration after a disconnect. This bit is useful for multi-threaded applications. The SYM53C710 was not capable of joining and winning arbitration immediately after a disconnect.

Wide SCSI Receive Bit – The Wide SCSI receive bit is asserted when the SYM53C770 detects a possible partial transfer at the end of a block move instruction. This residual byte is stored in the SCSI Wide Residue Data Register until the subsequent transfer. At this point the SYM53C770 can determine if the byte was “residual” data, valid data for a subsequent transfer, or overrun data. This byte is combined with another byte during the subsequent receive operation if the data is valid.

This bit makes it possible to chain data within multiple block move instructions. If a move instruction ends on an odd byte boundary the next move instruction provides an additional byte, allowing a word transfer.

Vendor Unique Enhancements bit 1 (VUE1) – VUE1 indicates whether the group code field in the SCSI instruction is standard or vendor unique.

Wide SCSI Send Bit – This bit is asserted at the start of a Wide SCSI send operation. If the transfer ends on an odd byte boundary, the bit remains asserted at the end of the transfer. This indicates that the low order byte of the SCSI Output Data Latch Register contains the last byte from the current send operation. The low order byte is combined with the high order byte of the subsequent send operation.

This bit makes it possible to chain data within multiple block move instructions. If a move instruction ends on an odd byte boundary, the next move instruction provides the high order byte. This allows a word transfer.

Chained Mode Bit – The chained mode bit allows chained block move instructions. The SCRIPTS processor automatically sets the bit on execution of a chained block move instruction. The processor resets the bit on execution of a regular block move SCRIPTS instruction.

When this bit is set and a data transfer ends on an odd byte boundary the SYM53C770 stores the last byte. During a receive, the bit is stored in the SCSI Wide Residue Data Register. During a send it is stored in the SCSI Output Data Latch Register. This byte is combined with the first byte from the subsequent transfer so that a wide transfer can be completed.

SCSI Disconnect Unexpected Bit – The SCSI disconnect unexpected bit should be asserted if the SYM53C770 is not expecting the SCSI bus to enter the bus free phase. The SYM53C770 automatically sets this bit when it is selected, reselected, performs a selection, or a reselection. The bit only has meaning in initiator mode.

The SYM53C770 uses this bit to determine if the disconnect was expected. If the chip enters a bus free phase and the bit is set, an unexpected disconnect error is generated in the SCSI Interrupt Status Register Zero.

Enable Wide SCSI Bit – The Wide SCSI bit enables 16-bit data transfers over the SCSI bus when set. The bit is cleared for 8-bit only data transfers.

Wide SCSI operation allows the SYM53C770 to double its data transfer rate across the SCSI bus.

Selection and Reselection Control Bits – The selection enable bit should be asserted when the SYM53C770 is required to respond as a target. The reselection enable bit (SCID, bit 6) should be asserted when it is required to respond as an initiator. There are also status and interrupt bits indicating whether or not the SYM53C770 has been selected or reselected. The SYM53C710 contains only one bit to indicate whether the chip had been selected/reselected.

The selection or reselection enable bit allows the SYM53C770 to respond as either an initiator or a target device. For example, if only selection is enabled, the SYM53C770 cannot be reselected as an initiator. The status and interrupt bits can be polled to allow execution of the appropriate target or initiator SCRIPTS. These bits also make it possible to determine whether the SYM53C770 has been selected or reselected.

General Purpose Input/Output Bits – These general purpose bits allow the SYM53C770 to detect the input signals of a connected device, or to enable attached ROM, RAM, or LEDs on a SYM53C770 board. The pins all have internal pull-ups.

The general-purpose input feature can be used to sense the SYM53C770 chip ID or board configuration at power up. A register to Register Move instruction may be used to move the sensed value into the appropriate register.

SCSI Selector ID Valid Bit/Encoded Destination SCSI ID Bits – The SCSI selector valid ID bit is automatically set when two SCSI IDs are detected on the bus during a bus-initiated selection or reselection. The encoded destination ID bits contain the ID of the initiator selecting the SYM53C770, or the ID of the target re-selecting the SYM53C770. The destination ID is valid when the selector ID is set.

This bit enhances the development of multi-threaded I/O SCRIPTS. The ability to detect the ID of the selector/reselector eases the chip's ability to support disconnects

SCSI Data Parity One Signal – The SCSI data parity one signal represents the parity on the high order byte lane. The parity signal is unlatched and can change at any time.

The SCSI Parity signal is used to detect parity errors on the upper byte lane during wide data transfer.

Last Disconnect Bit – The last disconnect bit is used in conjunction with the connected bit in the SCSI Control Register One to determine if a disconnect and subsequent selection or reselection of the SYM53C770 has occurred. If the connected bit is asserted and the last disconnect bit is asserted, a disconnect has occurred. The bit is also asserted at chip reset, indicating a disconnect state.

The last disconnect bit, in conjunction with the connected bit, notifies the SYM53C770 that a disconnect has occurred and that it is again connected to a SCSI device. Every time the last disconnect bit is set after execution of a CHMOV instruction, it indicates that a disconnect occurred since the prior CHMOV instruction.

DIFFSENSE SENSE Bit – The DIFFSENSE SENSE bit indicates whether the proper cable type has been connected for differential operation. It prevents damage to single ended devices and differential transceivers.

Latched SCSI Data Parity One Signal – The latched SCSI data parity one signal represents the odd parity of the high order byte in a 16-bit data transfer. The data is latched in the most significant byte of the SCSI Input Data Latch Register. It detects parity errors on the upper byte lane in 16-bit data transfers.

SCSI Output Data Latch Most Significant Byte Full – This bit is asserted when the high order byte is written to the SCSI Output Data Latch Register (SODL) during a synchronous or an asynchronous SCSI send operation. The bit is deasserted when the byte is transferred from the SODL register to the SCSI bus during an asynchronous send. It is also deasserted when the byte is transferred to the internal SCSI Output Data Register during a synchronous send.

This bit determines if the high order byte remains in the SCSI Output Data Latch Register when the chip halts a data transfer operation. The allows data pointer restoration after an interrupt.

SCSI Output Data Register Most Significant Byte Full – This bit is asserted when the high order byte is written to the SCSI Output Data Register during a synchronous SCSI send operation. The bit is deasserted when the byte is transferred to the SCSI bus during a synchronous send operation.

This bit determines if the high order byte remains in the SCSI Output Data register when the chip halts a data transfer operation. This allows data point restoration after an interrupt.

SCSI Input Data Latch Most Significant Byte Full – This bit is asserted when the high order byte is written to the SCSI Input Data Latch Register (SIDL) during an asynchronous SCSI receive operation. The bit is deasserted when the byte is transferred to the SIDL register to the DMA FIFO.

This bit determines if there is a higher order byte in the SIDL register. This determination allows the SCRIPTS processor to finish transferring data into memory after an interrupt.

Interrupt on the Fly Bit – This bit can be asserted by an interrupt instruction during SCRIPTS execution. SCRIPTS programs do not halt when the interrupt occurs. The interrupt must be serviced by reading the Interrupt Status Register only.

This bit notifies of a service routine, running on the main processor, while the SCRIPT processor is still executing a SCRIPTS program.

Semaphore Bit – The semaphore bit can be set by the SCRIPTS processor using a SCRIPTS register write. The bit may also be set by an external processor when the SYM53C770 is executing a SCRIPT.

This bit enables the SYM53C770 to notify the external processor of a predefined condition while SCRIPTS are running. The processor may also notify the SYM53C770 of a predefined condition and the SCRIPTS processor may take action while SCRIPTS are executing.

Generate Receive Parity for Pass Through Bit – When this bit is set and the SYM53C770 is in parity pass through mode, parity received on

the SCSI bus does not pass through the DMA FIFO. Parity is generated as data enters the DMA FIFO, eliminating the possibility of passing bad SCSI parity through the host bus.

Host Parity Check Enable bit – Asserting this bit enables parity checking during slave write and DMA read execution. On power up, this bit is disabled, allowing the SYM53C770 to function properly with systems that do not support parity.

Shadow Register Test Mode – Asserting this bit allows the user to read and retrieve data from the Shadowed Temporary Stack (TEMP) and Data Structure Address Registers (DSA).

These registers are “shadowed” because both are overwritten during a memory to memory move operation. The TEMP and DSA registers contain the base address used for all table indirect calculations and the instruction address pointer respectively.

SCSI Data Bus High Impedance Mode – Asserting this bit places the SCSI data bus and parity lines in a high-impedance state. It facilitates functional or burn-in testing.

Enable Host Parity Error Interrupt – Asserting this bit generates a hardware interrupt from the SYM53C770 when a parity error is detected at the host interface. If the bit is cleared the external IRQ/ signal is not asserted.

This bit notifies the main processor that a parity error has occurred at the host interface.

Host Bus Width Equal to 16-Bits – When this bit is set the SYM53C770 host interface converts to a 16 bits. The default mode is 32 bits at the host interface.

Note: Data lines 31-16 must be tied to data lines 15-0).

Bus Mode Bit – Asserting this bit redefines the function code pins. The bit should only be asserted when the SYM53C770 is in 80386sx or 80386dx mode or is not used in a native 68030 or 68040 environment. FC0 remains unaffected and provides a data control signal. FC1 becomes reserved and FC2 becomes an input to allow preview of next addresses.

This allows the SYM53C770 to interface to the EISA bus with greater ease, to the EISA bus.

Size Throttle Enable Bit – This bit causes the SYM53C770 to relinquish bus ownership every time the transfer size changes. It allows the SYM53C770 to interface to host buses that do not allow size changes within a bus ownership.

Handshake-to-Handshake Timer Expired Interrupt Enable – When this bit is set, the SYM53C770 generates a hardware interrupt on expiration of the handshake-to-handshake timer. The time measured is the SCSI REQuest to REQuest or ACKnowledge to ACKnowledge period. The time-out period is programmed in the SCSI Timer Register ZERO, bits 7-4. Possible time-out values range from 100 microseconds to greater than 1.6 seconds. If the bit is cleared the external IRQ/signal is not asserted.

General Purpose Timer Expired Interrupt Enable – When this bit is set, the SYM53C770 generates a hardware interrupt on expiration of the general-purpose timer. The time-out period is programmed in the SCSI Timer Register One, bits 3-0. Possible time-out values range from 100 microseconds to greater than 1.6 seconds. If the bit is cleared the external IRQ/ signal is not asserted.

SCSI Interrupt Status Zero Register – This register returns the status of the various interrupt conditions that can occur in the SCSI Interrupt Enable Register Zero. Each bit value asserted indicates occurrence of the corresponding interrupt condition. The bits are polled since the external IRQ/ signal is not asserted.

SCSI Interrupt Status Register One – This register returns the status of the various interrupt conditions that can occur in the SCSI Interrupt Enable Register One. Each bit value asserted indicates occurrence of the corresponding interrupt condition. The bits are polled since the external IRQ/ signal is not asserted.

SCSI Wide Residue Data Register – This register contains a residual byte, the first byte of a subsequent transfer, or an overrun data byte. If an Ignore Wide Residue message is not received the wide residue data becomes part of the next data transfer.

Response ID Zero and Response ID One Registers – These registers contain the selection or reselection IDs that the chip responds to on the SCSI bus. Each bit represents one possible ID.

These registers allow the SYM53C770 to respond to more than one ID. However, the chip can arbitrate with only one ID value in the SCID register.

Programmable Select/Reselect Time-out Timer – This select/reselect timer, if activated, interrupts the SYM53C770 if the chip has not been selected or reselected within a user defined time period. The timer is programmable from 100 microseconds to 25.6 seconds. The SYM53C710 used the Selection/Reselection Timer and the time-out period was fixed at 250 ms.

This select/reselect timer is provided so that the system does not have to furnish it in software. The select/reselect time-out period required by the SCSI specification is 250 ms.

Programmable Handshake Time-out Timer – This handshake timer, if activated, interrupts the SYM53C770 if the chip has not monitored a transfer within a predefined time period. The time measured is the SCSI REQuest to REQuest or ACKnowledge to ACKnowledge period. The timer is programmable from 100 microseconds to 25.6 seconds. The SYM53C710 used the Section/Reselection Timer and the time-out period was fixed to be 250 ms.

The handshake timer is provided so that the system does not have to furnish it. The interrupt informs the SYM53C770 that the connected SCSI device is not responding.

Programmable General Purpose Timer – This general-purpose timer, if activated, interrupts the SYM53C770 after expiration of a predefined time period. The timer is programmable from 100 microseconds to 1.6 seconds.

The timer may be used to limit the time the SYM53C770 spends on or off the bus. Once the interrupt occurs, a SCRIPT Disconnect instruction may be executed to free the bus or a Select instruction may be issued to get back on the bus.

SCSI Synchronous Offset Maximum Bit – This bit indicates that the current synchronous SCSI REQ/ACK offset is the maximum specified by bits 3-0 in the SCSI Transfer register. This bit is not latched and may change at any time. The SYM53C710 incorporated this function in the CTEST2 register, bit 5.

This bit is used in low level synchronous SCSI operations. When this bit is set and the SYM53C770 is a target, the chip is waiting for the initiator to ACKnowledge the data transfers. If the SYM53C770 is an initiator, then the target has sent the offset number of REQuests.

SCSI Synchronous Offset Zero Bit – This bit indicates that the current synchronous SCSI REQ/ACK offset is zero. It is not latched and may change at any time. The SYM53C710 incorporated this function in the CTEST2 register, bit 5.

This bit is used in low level synchronous SCSI operations. When this bit is set and the SYM53C770 is an initiator, the chip is waiting for the target to REQuest data transfers. If the SYM53C770 is a target then the initiator has sent the offset number of ACKnowledges.

Arbitration Priority Encoder Test Bit – This bit is always asserted when the SYM53C770 exhibits the highest priority ID asserted on the SCSI bus during arbitration. It is primarily used for chip level testing but it may be used during low level mode to determine if the SYM53C770 has won arbitration.

Selection Response Logic Bit – This bit is asserted when the SYM53C770 is available for selection or reselection. This does not take into account the bus settle delay of 400 ns. This bit is used for functional test and fault purposes.

Extended REQ/ACK Filtering Bit – Asserting this bit provides additional filtering on the deasserting edge of the REQ/ and ACK/ signals. The filter should not be used during fast SCSI transfers, greater than 5 Mbytes/s. Asserting this bit filters out glitches which may be interpreted by the SYM53C770 as assertions of the REQ/ and ACK/ signals.

Always Wide SCSI Bit – When this bit is asserted, all SCSI information transfers are executed in 16-bit mode. In other words, all the phases

supported by the SCRIPTS language (message, data, instruction and status) are performed in 16-bit mode.

This bit should normally be deasserted since 16-bit wide message, instruction, and status phases are not supported by the SCSI specifications. Also, this bit is not guaranteed to function properly with future Wide SCSI specifications.

SCSI Control Enable Bit – When this bit is asserted, all the SCSI control and data lines are driven regardless of whether the SYM53C770 is in target or initiator mode. This bit is primarily used for burn-in testing. This bit should not be set during normal operations, since contention on the SCSI bus may otherwise occur.

SCSI FIFO Test Read and Write Bus – These bits place the SCSI core into a test mode which allows easy reads and writes to the SCSI FIFO. These bits provide additional testing and system diagnostics.

SCSI FIFO Test Mode Bit – Asserting this bit places the SYM53C770 in a test mode which allows easy reads and writes to the FIFO. This allows FIFO functionality testing.

Clear SCSI FIFO Bit – Asserting this bit allows the user to clear the flags indicating that the FIFO is full. This allows the user to clear the FIFO.

Timer Test Mode Bit – Asserting this bit allows the user to test the SYM53C770 timers. Setting the bit starts the selection time-out, general purpose, and handshake-to-handshake timers. Use of this bit facilitates functional testing and increases fault coverage.

16-Bit System – Asserting this bit allows the SYM53C770 to consider 16-bit selection attempts. If parity checking is enabled parity is checked on the high and low order byte lanes.

Wide selection attempts are considered whereas 8-bit only selection attempts may be ignored due to bad parity since the high order byte lane is not driven.

Disable Single Initiator Response Bit – When this bit is asserted, the SYM53C770 ignores all bus-initiated selection attempts which employ the single initiator option of SCSI-1. This bit may be asserted in SCSI-2

systems so that a single bit error on the SCSI bus will not be interpreted as a single initiator response by the SYM53C770.

Halt SCSI Clock Bit – When this bit is asserted, the SCSI clock stops in a glitchless manner. Deasserting the bit starts the clock without glitches.

This bit may be used for test purposes or to lower I_{DD} during a power down mode. SCSI registers must be re-initialized upon power-up.

SCSI Input Data Latch Bits – Bits 15 through 8 in the SCSI Input Data Latch Register were added to accommodate the chip's Wide SCSI data transfer capability. This register is utilized during asynchronous data receive. The addition of these bits allows the SYM53C770 to concurrently receive 16 bits of data.

SCSI Output Data Latch Bits – Bits 15 through 8 in the SCSI Output Data Latch Register were added to accommodate the chip's Wide SCSI data transfer capability. This register is utilized during synchronous and asynchronous data send. The addition of these bits allows the SYM53C770 to concurrently send 16 bits of data.

SCSI Bus Data Lines Bits – Bits 15 through 8 in the SCSI Bus Data Lines Register were added to allow reading the extra data bits on the SCSI bus. This data is not latched and can change while being read. The addition of these bits makes it possible to concurrently view all the SCSI data lines.

SCRATCH B and SCRATCHC C-J – The SCRATCH register is a second general-purpose user definable 32-bit read/write register. It is a general purpose holding register.

6.2 Deleted Registers/Bits

Table 3 summarizes the registers and bits that were deleted when the SYM53C770 was designed.

Table 3 Deleted Registers and Bits

Registers/Bits	SYM53C710	SYM53C770
Start SCSI Receive Operation bit	SCNTL1, bit 0	Not Supported
Start SCSI Send Operation bit	SCNTL1, bit 1	Not Supported
Enable Selection and Reselection	SCNTL1, bit 5	Not Supported
SCSI Destination ID bits 7-4	SDID bit 7-4	Not Supported
SCSI Chip ID bits 7-4	SCID bit 7-4	Not Supported
SCSI Offset Compare bit	CTEST2, bit 5	Not Supported
SCSI FIFO Write Enable bit	CTEST4, bit 3	Not Supported
DACK/ bit	CTEST5, bit 0	Not Supported
DREQ/ bit	CTEST5, bit 1	Not Supported
EOP bit	CTEST5, bit 2	Not Supported
Chip Test Register Seven	CTEST7	Not Supported

Note: Addresses are Little Endian.

6.3 Moved Registers/Bits

Table 4 summarizes the registers and bits that were moved when designing the SYM53C770.

Table 4 Moved Registers and Bits

Registers/Bits	SYM53C710	SYM53C770
SCSI Destination ID Register (SDID)	Address 02h	Address 06h
SCSI Interrupt Enable Register (SIEN)	Address 03h	Address 40h
SCSI Synchronous Transfer Period	SXFER, bits 6-4	SXFER, bit 7-5
Disable Halt on Parity Error or ATN bit	SXFER, bit 7	SCTRL1, bit 5
SCSI Output Data Latch Register (SODL)	Address 06h	Address 54-55h
SCSI Output Control Latch Register (SOCL)	Address 07h	Address 09h
SCSI Input Data Latch Register (SIDL)	Address 09h	Address 50-51h
SCSI Bus Data Line Register (SBDL)	Address 0Ah	Address 58-59h
Synchronous SCSI Clock Frequency	SBCL, bits 1-0	SCNTL3, bit 6-4
SCSI RST/ Received bit	SSTAT0, bit 1	SIST0, bit 1
Unexpected Disconnect bit	SSTAT0, bit 2	SIST0, bit 2
SCSI Gross Error bit	SSTAT0, bit 3	SIST0, bit 3
Function Complete bit	SSTAT0, bit 6	SIST0, bit 6
Phase Mismatch or ATN/ Active bit	SSTAT0, bit 7	SIST0, bit 7
SCSI Status Register One	SSTAT1	SSTAT0
SCSI Status Register Two	SSTAT2	SSTAT1
Chip Test Register Zero (CTEST0)	Address 14h	Address 18h
Data Transfer Direction bit	CTEST0, bit 0	CTEST2, bit 7
Chip Test Register One (CTEST1)	Address 15h	Address 19h
Chip Test Register Two (CTEST2)	Address 16h	Address 1Ah

Table 4 Moved Registers and Bits

Registers/Bits	SYM53C710	SYM53C770
SCSI FIFO Parity (bits 7-0) bit	CTEST2, bit 4	STEST1, bit 0
Chip Test Register Three (CTEST3)	Address 17h	Address 1Bh
Chip Test Register Four (CTEST4)	Address 18h	Address 21h
SCSI Loopback Enable bit	CTEST4, bit 4	STEST2, bit 4
SCSI High Impedance Mode bit	CTEST4, bit 5	STEST2, bit 3
Chip Test Register Five (CTEST5)	Address 19h	Address 22h
Reset SCSI Offset bit	CTEST5, bit 5	STEST2, bit 6
Chip Test Register Six (CTEST6)	Address 1Ah	Address 23h
Transfer Type bit	CTEST7, bit 1	CTEST0, bit 1
Even Parity - Host Bus bit	CTEST7, bit 2	CTEST0, bit 2
DMA FIFO Parity bit	CTEST7, bit 3	CTEST0, bit 3
Snoop Control bits 1-0	CTEST7, bit 6-5	CTEST0, bits 6-5
Cache Burst Disable bit	CTEST7, bit 7	CTEST0, bit 7
Chip Test Register Eight	CTEST8	CTEST3
Interrupt Status Register (ISTAT)	Address 21h	Address 14h
Longitudinal Parity Register	LCRC 23h	SLPAR 44h
Enable Low Level SCSI Mode	DCNTL, bit 3	STEST2, bit 0
Clock Frequency bits	DCNTL, bit 7-6	SCNTL 3, 2-0

Note: Addresses are Little Endian.

Notes