System Engineering Notes
No. 840
SYM53C710, SYM53C720 False Bus Request
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This engineering note provides information on how to identify a false bus request, and how to create a Bus Request signal that is always valid. A false bus request is defined as the condition when the SYM53C7X0 requests the host bus but does not use it. The information in this note is for designs that cannot accommodate false host bus requests. If your system can handle the false bus request condition, disregard this note. The information in this engineering note applies to SYM53C710 and SYM53C720 products with the following part numbers: 609-3400654, 609-3400546, and 609-3400669.
The SYM53C7X0 will periodically assert the Bus Request (BR/) signal and simultaneously receive a SCSI interrupt. When this happens, the chip will wait for the Bus Grant (BG/) signal to compete the normal bus arbitration handshake. The chip no longer wants host bus access - after receiving BG/ the chip will take bus ownership for one BCLK, deassert the BR/, MASTER/ and all control lines (after the one BCLK), but will not assert Transfer Start (TS/), the signal that indicates a bus cycle is starting. The chip will return the DMA bus to a Bus Free state, allowing other bus masters to take control. The chip will generate the SCSI interrupt, which the system should service, and then continue with its normal operation. The attached timing diagrams show a normal host bus access (Figure 1) and a false bus request (Figure 2).

To differentiate between a true request and a false request the SC0 (Snoop Control 0) pin can be used on the SYM53C710 or SYM53C720. When bit 0 of CTEST8 is set, Bus Snooping is enabled and SC0 is a look-ahead copy of the internal bus request signal. The Figure 2 shows, when snooping is enabled and a false bus request occurs the SC0 pin will NOT be asserted at the time BR/ is asserted.

If the processor is unable to handle a false bus request, such as when it is looking for a TS/ signal, external logic may be required. To create a bus request that is always valid, BR/ can be inverted and then NANDED with the SC0 signal. Bus snooping must be enabled. Because the BR/ signal is an interlocked handshake with BG/, logic must be implemented to create a BG/ signal that will complete the handshake in case of a false bus request. The bus will then return to a Bus Free state, allowing normal arbitration by other devices.

This logic must do four things:

1. Logically filter out the false bus request seen by the system.
2. Assert a BG/ signal to the SYM53C7X0.
3. Ensure that the signals driven during the one BCLK ownership do not interfere with normal system operations.
4. Deassert the BG/. (The BG/ signal need only be 1 BCLK wide).

Note: When implementing the logic to create an “always valid” bus request, it is essential that the SC0 not be delayed. Therefore, the BR/ signal must be the signal of choice to be inverted and then “NANDED” with the SC0 signal (See Figure 3).

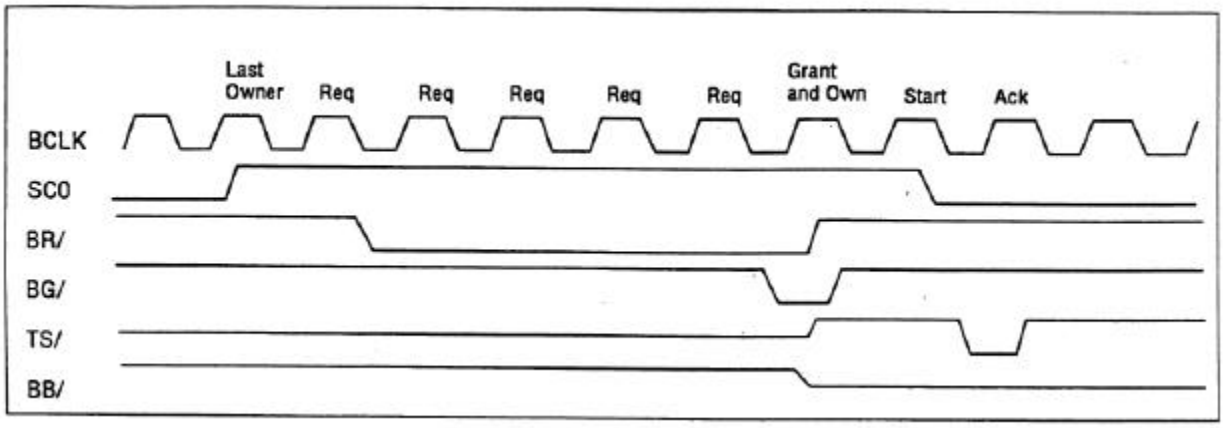

Figure 1. Normal Bus Request

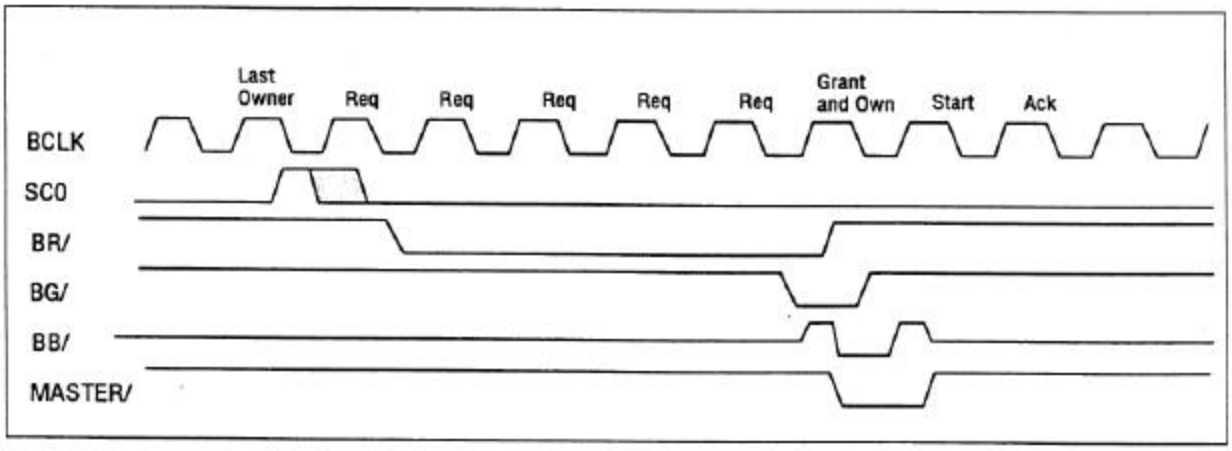

Figure 2. False Bus Request

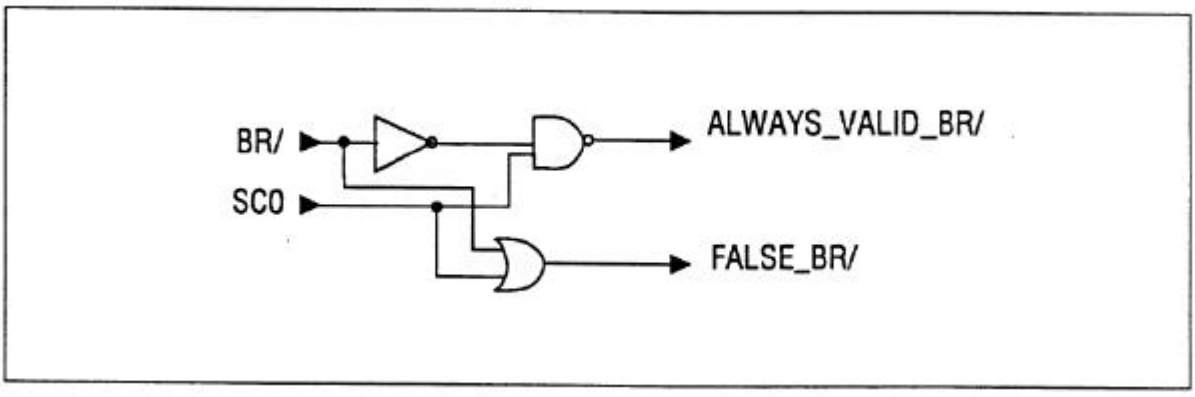

Figure 3. Circuit to Create "Always Valid" Bus Request